

UNITED STATES DEPARTMENT OF COMMERCE United States Patent and Trademark Office Address: COMMISSIONER FOR PATENTS P.O. Box 1450 Alexandria, Virginia 22313-1450 www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO
09/891,316	06/27/2001	Shotaro Uchida	210093US2S	1655
22850 7	7590 10/09/2003		EXAMINER	
OBLON, SPIVAK, MCCLELLAND, MAIER & NEUSTADT, P.C.			IM, JUNGHWA M	
1940 DUKE STREET ALEXANDRIA, VA 22314			ART UNIT	PAPER NUMBER
			2811	
			DATE MAILED: 10/09/2003	

Please find below and/or attached an Office communication concerning this application or proceeding.

<u>. </u>		14				
	Application No.	Applicant(s)				
Office Action Commons	09/891,316	UCHIDA, SHOTARO				
Office Action Summary	Examin r	Art Unit				
TI MAN INO DATE A Chi	Junghwa M. Im	2811				
Th MAILING DATE of this communication app ars on the cover sh t with the correspondence address Period for Reply						
A SHORTENED STATUTORY PERIOD FOR REPLY THE MAILING DATE OF THIS COMMUNICATION. - Extensions of time may be available under the provisions of 37 CFR 1.13 after SIX (6) MONTHS from the mailing date of this communication. - If the period for reply specified above is less than thirty (30) days, a reply - If NO period for reply is specified above, the maximum statutory period wi - Failure to reply within the set or extended period for reply will, by statute, - Any reply received by the Office later than three months after the mailing earned patent term adjustment. See 37 CFR 1.704(b). Status	6(a). In no event, however, may a reply be time within the statutory minimum of thirty (30) days ill apply and will expire SIX (6) MONTHS from cause the application to become ABANDONE	nely filed s will be considered timely. the mailing date of this communication. D (35 U.S.C. § 133).				
1) Responsive to communication(s) filed on 30 J	<u>uly 2003</u> .					
2a) This action is FINAL . 2b) Thi	s action is non-final.					
3) Since this application is in condition for allowa						
closed in accordance with the practice under E Disposition of Claims	Ex parte Quayle, 1935 C.D. 11, 4	l53 O.G. 213.				
4) Claim(s) 8-26 is/are pending in the application.						
4a) Of the above claim(s) is/are withdrawn from consideration.						
5)⊠ Claim(s) <u>8-20</u> is/are allowed.						
6)⊠ Claim(s) <u>21-26</u> is/are rejected.						
7) Claim(s) is/are objected to.						
8) Claim(s) are subject to restriction and/or Application Papers	election requirement.					
9) The specification is objected to by the Examiner						
10) The drawing(s) filed on is/are: a) accepted or b) objected to by the Examiner.						
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).						
11) The proposed drawing correction filed on						
If approved, corrected drawings are required in reply to this Office action.						
12) The oath or declaration is objected to by the Examiner.						
Priority under 35 U.S.C. §§ 119 and 120						
13) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).						
a) ☐ All b) ☐ Some * c) ☐ None of:						
1. Certified copies of the priority documents have been received.						
2. Certified copies of the priority documents have been received in Application No						
Copies of the certified copies of the prior application from the International Bur See the attached detailed Office action for a list of the certified copies of the prior application.	eau (PCT Rule 17.2(a)).	-				
14) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).						
a) ☐ The translation of the foreign language prov 15)☐ Acknowledgment is made of a claim for domestic	visional application has been rec	eived.				
Attachment(s)						
1) Notice of References Cited (PTO-892) 2) Notice of Draftsperson's Patent Drawing Review (PTO-948) 3) Information Disclosure Statement(s) (PTO-1449) Paper No(s)	5) Notice of Informal F	/ (PTO-413) Paper No(s) Patent Application (PTO-152)				

Art Unit: 2811

DETAILED ACTION

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 22 and 25 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

Claims 22 and 25 recite that the first end of the inner frame covers the *Schottky diode* completely which aspect is not disclosed in the specification. The specification does not disclose any covering of the *diode region* by the inner lead frame. Note that Applicant recites a Schottky diode to use for a rectifier operation. Applicant discloses a formation of two MOSFET's on a package base.

The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 21-26 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one

Art Unit: 2811

skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

Claims 21 and 24 recite a first end of the inner lead frame connected to the main electrode covering a part of the Schottky diode, and the specification does not disclose a partial covering of the Schottky diode in a manner recited in the pending claim. On the contrary to Applicant's argument filed on June 27, 2003, Figures 7A-7C of the Application show a formation of two MOSFET's, not a formation of a MOSFET and a Schottky diode. And Fig. 7A shows that the inner lead frame (5) covers only the portion of the source electrodes (15₁, 15₂).

Claims 22, 23, 25 and 26 are dependent on the rejected base claims.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 24 and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Davis et al. (US 6144093), hereafter Davis, in view of Watanabe(US 5925926).

Regarding claim 24, Figure 3 of Davis shows a MOSFET 30 having a first source electrode 38 and a gate electrode 36 on an upper surface of the transistor chip, and a Schottky diode 32 formed between the source electrode and the drain electrode as shown in the circuit diagram Figure 6, the bottom surface of the Schottky diode and the drain of MOSFET are electrically connected to a pad 22 (col.3, lines 26-29) and an inner lead frame 28, a first end of

Art Unit: 2811

the inner lead frame being connected to the main electrode on a part of the diode region, a second end of the inner lead frame being connected to package lead.

In detail, Fig. 3 of Davis shows one end of inner lead portion is connected to the source electrode by a wire bond 42, also connecting the anode of the Schottky diode. Therefore, the wire bond from the end of the inner lead covers a portion of the Schottky diode region.

Also, note that Application simply recites a Schottky diode is connected parallel for a rectifier application. In addition, Fig. 4 of Davis shows the Schottky diode connected parallel to the MOSFET.

Davis shows a structure of the device substantially identical to the claimed invention except an inner lead frame made of a sheet metal. Watanabe discloses a semiconductor packaging device wherein the inner leads are made of sheet metal (col. 3, lines 1-2). It would have been obvious to one of ordinary skill in the art at the time of the invention to utilize the teaching of Watanabe for the device of Davis to have inner leads made of sheet metal since using sheet metal for the inner leads improves the mechanical strength for supporting a semiconductor chip.

Regarding claim 25, Figure 3 of Davis shows a MOSFET 30 having a first source electrode 38 and a gate electrode 36 on an upper surface of the transistor chip, and a Schottky diode 32 formed between the source electrode and the drain electrode as shown in the circuit diagram Figure 6, the bottom surface of the Schottky diode and the drain of MOSFET are electrically connected to a pad 22 (col.3, lines 26-29) and an inner lead frame 28, a first end of the inner lead frame being connected to the main electrode on a part of the diode region, a second end of the inner lead frame being connected to package lead.

Page 5

Application/Control Number: 09/891,316

Art Unit: 2811

In detail, Fig. 3 of Davis shows one end of inner lead portion is connected to the source electrode by a wire bond 42, also connecting the anode of the Schottky diode. Therefore, the wire bond from the end of the inner lead covers a portion of the Schottky diode region.

Also, note that Application simply recites a Schottky diode is connected parallel for a rectifier application. In addition, Fig. 4 of Davis shows the Schottky diode connected parallel to the MOSFET.

Davis shows a structure of the device substantially identical to the claimed invention except an inner lead frame made of a sheet metal. Watanabe discloses a semiconductor packaging device wherein the inner leads are made of sheet metal (col. 3, lines 1-2). It would have been obvious to one of ordinary skill in the art at the time of the invention to utilize the teaching of Watanabe for the device of Davis to have inner leads made of sheet metal since using sheet metal for the inner leads improves the mechanical strength for supporting a semiconductor chip.

Note that a semiconductor device does not comprises operation controlled by the electrodes which are part of the device. Rather, it would be obvious that the electrodes of the device would control electrical operation.

Regarding claims 23 and 26, Figure 8 of Davis shows an N-MOSFET. Alternatively it is obvious to use an NMOS in a semiconductor packaging device since an NMOS is one of the most commonly used semiconductor chip for an IC circuit.

Response to Arguments

Art Unit: 2811

Applicant's arguments filed June 27, 2003 have been fully considered but they are not persuasive.

First, Applicant mainly argues that the Application shows that a portion of the end of the inner lead partially covers the Schottky diode. As discussed extensively above in the Office Action, the specification of the Application merely shows that a portion of the end of the inner lead partially covers MOSFET's.

Second, parallel connection of Schottky diode to a transistor is not a part of the instant invention as stated extensively above in the Office Action. As is disclosed in the reference of Davis, a Schottky diode is configured parallel in an application circuit.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Junghwa M. Im whose telephone number is (703) 305-3998. The examiner can normally be reached on MON.-FRI. 8:30AM-5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (703) 308-2772. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

jmi September 30, 2003

Page 7